Claims 1, 3, 7 to 9, 18 to 21, 23 and 24 were rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi (U.S. 5,087,585). The rejection is again respectfully traversed both as to the claims as previously presented as well as to the claims as amended.

The invention herein resides broadly in the formation of one of a substrate or a device layer secured to a dielectric layer having interconnect structure disposed therein and extending therethrough to a surface of the dielectric layer and optional passive structure within the dielectric layer. The other of the substrate of device layer is then planarized along with the exposed surface of the dielectric layer. The exposed surface and the substrate or device layer are then bonded together after being aligned. There is no build-up of layer upon layer as is found in Hayashi. Furthermore, the interconnect structure is disposed within the dielectric layer. No such arrangement is found in Hayashi. Still further, any insulation buildup between the interconnect and the device to which interconnection is to be made is obviated by the application of a sufficiently high voltage across the insulation buildup, when necessary. It follows that the structures of Hayashi and the subject invention and the method of fabrication of the two are entirely different.

More specifically, and with reference to claim 1, this claim requires, among other steps, forming an electrically insulating layer having a pair of opposed outer faces, one of the outer faces disposed on the surface one of the substrate or the device wafer, the electrically insulating layer having an electrical interconnect structure disposed therewithin. No such step is taught or suggested by Hayashi either alone or in the combination as claimed. The insulative layer of Hayashi has no such arrangement. There is no interconnect in Hayashi and, in the event the non-refractory metal pool 18 is alleged to be such interconnect, which it is not, this element is not

disposed within the insulative layer 17. It follows that this element is not found in Hayashi either as presently or previously claimed.

Claim 1 further requires that a portion of the interconnect structure extend substantially to the one of the outer faces of the electrically insulating structure to make electrical contact with a device in at least one of the device wafer and the substrate. No such arrangement is found in Hayashi either alone or in the combination as claimed. The pool 18 of Hayashi is not disposed at a surface of the electrically insulating structure and is not shown as being connected to anything in the second layer thin film device 23 other than the layer itself.

Claim 1 yet further requires the step of then bonding the other of the outer faces of the electrically insulating layer to the surface of the other of the substrate or device wafer. No such step is taught or suggested by Hayashi either alone or in the combination as claimed. The order of the steps is specifically claimed and this order is nowhere taught or suggested by Hayashi.

Claim 3 depends from claim 1 and therefore defines over Hayashi for at least the reason provided above as to claim 1.

In addition, claim 3 further limits claim 1 by requiring that at least one of the device layer and the substrate include a bond region, the interconnect structure contacting the bond region. insulating layer sufficient to break down said portion of said electrically insulating layer while maintaining the integrity of the remainder of said SOI structure

Claim 7 requires, among other steps, provision of an SOI structure having a device layer having at least one of active or passive elements on a surface thereof, a substrate having at least one of active or passive elements on a surface thereof and an electrically insulating layer having an interconnect structure disposed within the electrically insulating layer and extending to a

surface of the electrically insulating layer. No such step is taught or suggested by Hayashi either alone or in the combination as claimed as discussed above with reference to claim 1.

Claim 7 further requires the steps of forming a substantially planar region on the surface of the device layer and the surface of the substrate and a region on the surface of the electrically insulating layer, interposing the electrically insulating layer between the device layer and the substrate with the planar region of the electrically insulating layer overlaying the substantially planar region on the at least one of the surface of the device layer and the surface of the substrate to make electrical contact with a device in at least one of the device wafer and the substrate and then bonding the surface to the other of the substrate wafer and device layer. No such steps are taught or suggested by Hayashi either alone or in the combination as claimed. Note the argument presented in connection with claim 1 as well as the fact that Hayashi has no electrically insulating layer having an interconnect structure which provides the claimed interconnect function in the electrically insulating layer bonded to one of the device layer or substrate after being affixed to the other of these elements in the manner claimed.

Claims 8 and 9 depend from claim 7 and therefore define patentably over Hayashi for at least the reasons presented above with reference to claim 7.

In addition, claim 8 further limits claim 7 by requiring the step of forming an electrical interconnect structure in the electrically insulating layer, the interconnect structure contacting at least one of the device layer and the substrate. No such step is taught or suggested by Hayashi either alone or in the combination as claimed. The interconnect structure of Hayashi is not "in the electrically insulating layer" but rather is external thereto.

Claim 9 further limits claim 7 by requiring the step of forming an electrical interconnect structure in the electrically insulating layer, the interconnect structure contacting both the device layer and the substrate. The argument applied as to claim 8 applies herein as well.

Claim 18 requires, among other steps, after providing a device layer having at least one of active or passive elements on a surface thereof and providing a substrate having at least one of active or passive elements on a surface thereof, providing a dielectric bonded to one of the device layer and the substrate having an interconnect disposed therein and extending to at least one surface thereof. No such step is taught or suggested by Hayashi either alone or in the combination as claimed.

Claim 18 further requires the step of then bonding the dielectric to the other of the device layer and the substrate to form an interface with the one of said device layer and the substrate and form an electrically conductive path across the interface to the interconnect. No such step or steps in the order claimed are taught or suggested by Hayashi.

Claims 19 to 21, 23 and 24 depend from claim 18 and therefore define patentably over Hayashi for at least the reason presented above with reference to claim 18.

In addition, claim 19 further limits claim 18 by requiring that the electrically conductive path contacts the other of the device layer and the substrate. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claims 20 and 21 further limit claims 18 and 19 by requiring that the electrically conductive path be an extension of said device layer. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claim 23 further limits claim 18 by requiring that the substrate be a semiconductor substrate. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claim 24 further limits claim 18 by requiring that the substrate comprise a semiconductor substrate and a dielectric. No such combination of steps in the order claimed is taught or suggested by Hayashi.

Claims 1 to 4, 7 to 9 and 18 to 24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi in view of Applicant's admitted prior art. The rejection is respectfully traversed.

The arguments presented above as to Hayashi is repeated since Applicant's admitted prior art does not overcome the demonstrated deficiencies in Hayashi. Claim 2, 4 and 22 are further patentable over the applied references since they depend from one of claim 1 or 18 as discussed above.

Claim 2 further limits claim 1 by requiring the step of applying a voltage across a portion of the electrically insulating layer sufficient to break down the portion of the electrically insulating layer while maintaining the integrity of the remainder of SOI structure. No such combination is taught or suggested by Hayashi, the admitted prior art or any proper combination thereof.

Claim 4 further limits claim 2 by requiring that at least one of the device layer and the substrate include a bond region, the interconnect structure contacting the bond region through the portion of the electrically insulating layer. No such combination is taught or suggested by Hayashi, the admitted prior art or any proper combination thereof.

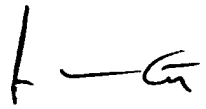
Claim 22 further limits claim 18 by requiring that the step of forming an electrically conductive path across the interface to the interconnect be formed by breakdown of the dielectric. No such combination is taught or suggested by Hayashi, the admitted prior art or any proper combination thereof.

Claims 25 and 26 depend from claims 1 and 7 respectively and therefore define patentably over Hayashi for at least the reasons presented above with reference to claims 1 and 7.

In addition, claims 25 and 26 further limit claims 1 and 7 by requiring the steps of forming an electrical insulation on at least one of the electrically insulating layer, the substrate or the device wafer insulating the interconnect structure from the device in the at least one of the device wafer and the substrate and applying a voltage across the electrical insulation to break down the electrical insulation an provide interconnection between the interconnect structure and the device. No such steps are taught or suggested by Hayashi either alone or in the total combination as claimed.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,



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1. A method of fabricating an SOI structure which comprises the steps of:

(a) providing a substrate having at least one of active or passive elements on a surface thereof;

(b) providing a device wafer having at least one of active or passive elements on a surface thereof;

C1

(c) forming an electrically insulating layer having a pair of opposed outer faces, one of said opposed outer faces disposed on a said surface of one of said substrate or said device wafer, said electrically insulating layer having an electrical interconnect structure disposed therewithin, a portion of said interconnect structure extending substantially to said one of said outer faces of said electrically insulating structure to make electrical contact with a device in at least one of the device wafer and the substrate; and

(c) then bonding the other of said outer faces of said electrically insulating layer to the said surface of the other of said substrate or device wafer.

7. A method of forming an SOI structure, comprising the steps of:

providing a device layer having at least one of active or passive elements on a surface thereof;

providing a substrate having at least one of active or passive elements on a surface thereof;

C2

providing an electrically insulating layer having an interconnect structure disposed therein and extending to a surface thereof;

forming a substantially planar region on said surface of said device layer and said surface of said substrate;

forming a substantially planar region on said surface of said electrically insulating layer;

interposing said electrically insulating layer between said device layer and said substrate with said planar region of said electrically insulating layer overlaying said substantially planar region on said at least one of said surface of said device layer and said surface of said substrate to make electrical contact with a device in at least one of the device wafer and the substrate; and

then bonding said planar surface of said electrically insulating layer to said overlying one of said substrate and said device layer.

25. The method of claim 1 further including the steps of forming an electrical insulation on at least one of said electrically insulating layer, said substrate or said device wafer insulating said interconnect structure from said device in said at least one of the device wafer and the substrate and applying a voltage across said electrical insulation to break down said electrical insulation an provide interconnection between said interconnect structure and said device.

26. The method of claim 7 further including the steps of forming an electrical insulation on at least one of said electrically insulating layer, said substrate or said device wafer insulating said interconnect structure from said device in said at least one of the device wafer and the substrate and applying a voltage across said electrical insulation to break down said electrical insulation an provide interconnection between said interconnect structure and said device.